AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method for controlling CPU speed transition, comprising:

receiving a System Management Interrupt (SMI) signal;

determining whether a bus master device is in an active state when the SMI signal is for performing CPU speed transition; and

canceling the CPU speed transition operation when the bus master device is determined to be in the active state and generating ~~at prescribed intervals~~ a retry SMI signal at prescribed intervals.

2. (Currently Amended) The method of claim 1, further comprising performing the CPU speed transition operation when the bus master device is not in the active state.

3. (Currently Amended) The method of claim 1, wherein the retry SMI signal generated at the prescribed intervals is one of a watchdog timer SMI signal and an embedded control SMI signal to retry the CPU speed transition operation.

4. (Original) The method of claim 3, wherein the determining comprises:

disabling occurrences of additional watchdog timer SMI signals when the received SMI signal is the watchdog timer SMI signal to retry the CPU transition operation; and

re-determining whether the bus master device is in the active state.

5. (Original) The method of claim 3, wherein the determining comprises:

disabling occurrence of additional embedded controller SMI signals when the received SMI signal is an embedded controller SMI signal to retry the CPU speed transition operation; and

re-determining whether the bus master device is in the active state.

6. (Original) The method of claim 3, wherein the determining comprises:

performing a prescribed operation corresponding to the received SMI signal when the received SMI signal is not an SMI signal for CPU speed transition, the watchdog timer SMI signal to retry the CPU speed transition operation or the embedded controller SMI to retry the CPU speed transition operation.

7. (Original) The method of claim 1, wherein the SMI signals are at least one of a hardware generated signal and an application program generated signal.

8. (Currently Amended) A portable computer, comprising:

a CPU configured to operate using at least two speeds;

a controller configured to perform a prescribed operation to transition between the at least two speeds of the CPU;

interrupt occurrence reason recognition means for recognizing an occurrence reason of an interrupt signal;

active state checking means for checking an active state of a predetermined device; and

interrupt generating means for creating a second interrupt signal to retry the prescribed operation for the CPU speed transition when the interrupt occurrence reason recognition means determines that a first interrupt signal is ~~created~~ for the CPU speed transition and the active state checking means determines that the predetermined device is in the active state, and the interrupt generating means creates the second interrupt signal based on a predetermined timer contained in the computer.

9. (Currently Amended) The portable computer of claim 8, wherein the first interrupt signal for the CPU speed transition is responsive to a change of CPU use amount, switching between AC adapter and battery power sources, reduction of battery lifetime, runtime setup of a user and temperature variation.

10. (Cancelled)

11. (Currently Amended) The portable computer of claim [[10]]8, wherein the predetermined timer ~~contained in the system is~~ comprises a watchdog timer or an inner timer of an embedded controller.

12. (Currently Amended) The portable computer of claim [[10]]8, wherein the second interrupt signal is created at intervals of a predetermined time determined by a system BIOS.

13. (Currently Amended) The portable computer of claim 8, wherein the predetermined device ~~is~~ comprises a bus master device.

14. (Currently Amended) The portable computer of claim 8, wherein the second interrupt is repeatedly generated until the CPU transition is performed, and wherein the portable computer ~~is~~ comprises a notebook computer.

15. (Currently Amended) An apparatus, comprising:

an interrupt receiver configured to receive interrupt signals; and

an interrupt generator coupled to the interrupt receiver and configured to generate a second interrupt signal to retry a prescribed operation needed for CPU speed transition when a first interrupt signal for the CPU speed transition is received and a bus master device is in an active state, and the interrupt generator generates the second interrupt signal based on a predetermined timer contained in the apparatus.

16. (Canceled)

17. (Currently Amended) The apparatus of claim [[16]]15, wherein the predetermined timer ~~contained in the system is~~comprises at least one of a watchdog timer and an inner timer of an embedded controller.

18. (Currently Amended) The apparatus of claim [[16]]15, wherein the second interrupt signal is created at intervals of a predetermined time determined by a system BIOS.

19. (Original) The apparatus of claim 15, wherein the apparatus is in a notebook computer.

20. (Original) The apparatus of claim 15, wherein the interrupt signals are one of hardware interrupts and software interrupts.

21. (Currently Amended) An article including a machine-readable storage medium containing instructions for controlling CPU speed transition in a computer system, said instructions, when executed in the computer system, ~~causing~~ cause the computer system to:

receive an System Management Interrupt (SMI) signal;

determine whether a bus master device is in an active state when the SMI signal is a first SMI CPU speed transition signal; and cancel the CPU speed transition operation when the bus master device is in the active state and generate an event at predetermined intervals~~ an event~~.

22. (Original) The article of claim 21, wherein the event is a second SMI CPU speed transition signal.

23. (Original) The article of claim 22, wherein the event is one of a hardware interrupt and a software interrupt.